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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,071	12/21/1999	TONGBI JIANG	MICRON.110A	6968

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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
ALCALA, JOSE H	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/471,071	JIANG, TONGBI	
	Examiner	Art Unit	
	José H Alcalá	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/31/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-23 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This non-final rejection is in response to amendment filed on 10/31/03.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8-23, are rejected under 35 U.S.C. 103(a) as being unpatentable over DiStefano et al. (US Patent No. 5,821,608) in view of Shiobara et al. (US Patent No. 5,340,851).

Regarding Claim 8, DiStefano teaches an integrated circuit package, comprising: a die (reference number 10); a die attach layer over the die (reference number 80'); and an array of solder balls (reference number 40) over the die attach layer. DiStefano further teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material, with a higher thickness and the desired material properties to compensate for thermal mismatch (column 6, lines 3-11).

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C. Shiobara teaches a thermosetting resin composition having a coefficient of thermal expansion of less than about 106 ppm/°C (See line 25 of Table 1). It would have been obvious to one of ordinary skill in

the art at the time the invention was made to combine the teachings of DiStefano and Shiobara, in order to make the die attach layer having a thermal expansion coefficient of less than about 106 ppm/°C, thus making the die attach layer easily workable, having improve adhesiveness, improved mechanical strength, hot-water resistance, and minimized water absorption.

Regarding Claim 9, DiStefano teaches a flexible tape (reference number 50) connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die (see Figure 1D).

Regarding Claim 10, DiStefano teaches that the die attach layer has a thickness of between about 5 and 7 mils (column 6, lines 9-11).

Regarding Claim 11, DiStefano as modified by Shiobara, teaches that the die attach layer is an epoxy modified with elastomeric material. See Column 5, lines 58-60 and column 14, lines 54-58.

Regarding Claim 12, DiStefano teaches that the array is a ball grid array (See Figure 1A).

Regarding Claim 13, DiStefano teaches that the array is a tape ball grid array (See Figure 1A and 1D).

Regarding Claim 14, DiStefano teaches that the array is a micro ball grid array (See Figure 1A).

Regarding Claim 15, DiStefano teaches an integrated circuit package, comprising: a die (reference number 10); a die attach layer over the die (reference

number 80'); and an array of solder balls (reference number 40) over the die attach layer. DiStefano further teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material, with a higher thickness and the desired material properties to compensate for thermal mismatch (column 6, lines 3-11).

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C, and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi. Shiobara teaches a thermosetting resin composition having a coefficient of thermal expansion of less than about 106 ppm/°C (See line 25 of Table 1) and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi (See line 23 of Table 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of DiStefano and Shiobara, in order to make the die attach layer having a thermal expansion coefficient of less than about 106 ppm/°C and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi, thus making the die attach layer easily workable, having improve adhesiveness, improved mechanical strength, hot-water resistance, and minimized water absorption.

Regarding Claim 16, DiStefano teaches a flexible tape (reference number 50) connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die (See figure 1D).

Regarding Claim 17, DiStefano teaches a first level integrated circuit package comprising: a first level package including a chip (reference number 10); an array of

solder balls (reference number 40), an adhesive layer (reference number 80) between the chip and the array of solder balls, and a flexible tape (reference number 50) connecting the array to the chip wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip. DiStefano further teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material, with a higher thickness and the desired material properties to compensate for thermal mismatch (column 6, lines 3-11).

The limitation that the array of solder balls is: "for connecting the first level package to a second level package", is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 200 ppm/°C. Shiobara teaches a thermosetting resin composition having a coefficient of thermal expansion of less than about 200 ppm/°C (See line 25 of Table 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of DiStefano and Shiobara, in order to make the die attach layer having a thermal expansion coefficient of less than about 106 ppm/°C, thus making the die attach layer easily workable, having improve adhesiveness, improved mechanical strength, hot-water resistance, and minimized water absorption.

Regarding Claim 18, DiStefano teaches that the tape connects the array to the chip using μBGA technology (See Figure 1A).

Regarding Claim 19, DiStefano as modified by Shiobara teaches that the die attach layer has a coefficient of thermal expansion of less than about 150 ppm/°C (See line 25 of Table 1 of Shiobara).

Regarding Claim 20, DiStefano as modified by Shiobara teaches that the die attach layer has a coefficient of thermal expansion of less than about 100 ppm/°C (See line 25 of Table 1 of Shiobara).

Regarding Claim 21, DiStefano teaches a first level integrated circuit package comprising: a first level package including a chip (reference number 10); an array of solder balls (reference number 40), an adhesive layer (reference number 80) between the chip and the array of solder balls, and a flexible tape (reference number 50) connecting the array to the chip wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip (See Figure 1D). DiStefano further teaches that it is desirable to have the die attach layer be a thermoset or thermoplastic material, with a higher thickness and the desired material properties to compensate for thermal mismatch (column 6, lines 3-11)..

The limitation that the array of solder balls is: "for connecting the first level package to a second level package", is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus

satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

DiStefano fails to explicitly teach that the die attach layer has a coefficient of thermal expansion of less than about 200 ppm/°C, and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi. Shiobara teaches a thermosetting resin composition having a coefficient of thermal expansion of less than about 200 ppm/°C (See line 25 of Table 1) and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi (See line 23 of Table 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of DiStefano and Shiobara, in order to make the die attach layer having a thermal expansion coefficient of less than about 200 ppm/°C and a modulus of elasticity of less than about 126 ksi, and greater than about 10 ksi, thus making the die attach layer easily workable, having improve adhesiveness, improved mechanical strength, hot-water resistance, and minimized water absorption.

Regarding Claim 22, DiStefano as modified by Shiobara teaches that the die attach layer has a modulus of elasticity of greater than about 50 ksi (See line 23 of Table 1).

Regarding Claim 23, DiStefano as modified by Shiobara teaches that the die attach layer has a modulus of elasticity of greater than about 100 ksi (See line 23 of Table 1).

4. Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khandros et al. (US Patent No. 5,347,159) in view of Shiobara et al. (US Patent No. 5,340,851).

Regarding Claim 25, Khandros teaches an integrated circuit package, comprising: a flexible substrate (reference number 88); a chip (reference number 20); a plurality of conductive terminals (reference number 91) on the substrate; a plurality of conductive leads (reference number 48) electrically connecting the conductive terminals to the chip; and a compliant material (reference number 64) between the chip and the substrate. In addition, Khandros teaches that the compliant material is an elastomer compliant layer with elastic properties comparable to those of soft rubber (column 8, lines 8-15), but fails to explicitly teach that it has modulus of elasticity of less than about 126 ksi and a coefficient of thermal expansion of less than about 200 ppm/°C.

Shiobara teaches a compliant layer having a coefficient of thermal expansion of less than about 200 ppm/°C (See line 25 of Table 1) and a modulus of elasticity of less than about 126 ksi, (See line 23 of Table 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Khandros and Shiobara, in order to make the compliant material layer having a thermal expansion coefficient of less than about 200 ppm/°C and a modulus of elasticity of less than about 126 ksi, thus making the compliant layer easily workable, having improved mechanical strength, hot-water resistance, and minimized water absorption.

Regarding Claim 26, Khandros teaches that the plurality of conductive terminals includes an array of solder balls (reference number 91).

Regarding Claim 27, Khandros teaches that the plurality of conductive leads (reference number 48) includes TAB leads .

5. Claim 28, is rejected under 35 U.S.C. 103(a) as being unpatentable over Khandros et al. (US Patent No. 5,347,159) in view of Shiobara et al. (US Patent No. 5,340,851) as applied above for claim 25, and further in view of Di Stefano (US Patent No. 5,821,608).

Regarding Claim 28, Khandros as modified by Shiobara teaches all the elements as stated supra for claim 25, but fails to explicitly teach that the flexible substrate is a polyimide. DiStefano teaches that the substrate is made of a polyimide (column 5, line 23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the flexible substrate made of a polyimide, in order to improve the flexibility of the package device. See In re Leshin, 125 USPQ 416.

Response to Arguments

6. Applicant's arguments with respect to the rejection under 35 U.S.C. § 112, first paragraph are persuasive. Therefore, the rejection under 35 U.S.C. § 112, first paragraph has been withdrawn.

7. Applicant's arguments, see pages 7-8, filed on 10/31/03, with respect to the rejection(s)of claim(s) 25-28 under Khandros et al. (US Patent No. 5,347,159) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made based Khandros et al. (US Patent No. 5,347,159) in view of Shiobara et al. (US Patent No.

5,340,851) for claims 25-27, and further in view of Di Stefano (US Patent No. 5,821,608) for claim 28.

8. Applicant's arguments, see pages 8-10, filed on 10/31/03, with respect to the rejection(s)of claim(s) 8-23 under DiStefano et al. (US Patent No. 5,821,608) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made based on DiStefano et al. (US Patent No. 5,821,608) in view of Shiobara et al. (US Patent No. 5,340,851).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach some of the elements of the instant claimed invention or some similar arrangements of the elements: Ito et al. (US Patent No. 5,157,061), Kreuz et al. (US Patent No. 5,196,500), Carson (US Patent No. 6,468,830), Wark (US Patent No. 5,817,540) and DiStefano (US Patent No. 6,127,724).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to José H Alcalá whose telephone number is (571) 272-1926. The examiner can normally be reached on Monday to Friday, first Friday off.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHA

David A. Zarneke
Primary Exam
AU 2827
2/20/04